

# **Exhibit 1**

**I R E L L   &   M A N E L L A   L L P**

A REGISTERED LIMITED LIABILITY LAW PARTNERSHIP  
INCLUDING PROFESSIONAL CORPORATIONS

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November 10, 2022

**VIA E-MAIL**

Michael R. Rueckheim  
Winston & Strawn LLP  
255 Shoreline Drive, Suite 520  
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[MRueckheim@winston.com](mailto:MRueckheim@winston.com)

Re: *Netlist, Inc. v. Micron Technology, Inc. et al*, 22-cv-203-JRG-RSP (E.D. Tex.)

Dear Mr. Rueckheim:

We write regarding Micron's obligation to produce relevant documents (including materials, tangible things, and information) under the Court's Discovery Order and the Federal and Local Rules. This letter provides examples of highly relevant documents within the scope of Micron's discovery duties. Netlist, Inc. ("Netlist") specifically requests that these and all other relevant documents be produced. The list below is intended to help Micron categorize information that needs to be produced and does not in any way waive, limit, or alter any discovery obligations. Micron should produce all documents and things as will be required by the Court's Discovery Order, Docket Control Order, and Local Rules. As discovery is ongoing, Netlist reserves the right to supplement this list of examples.

Please confirm that these documents will be produced by November 21, 2022.

**Definitions**

1. The terms "Micron" (or "You" or "Your") shall mean and include Micron Technology, Inc. ("Micron Technology"), Micron Semiconductor Products, Inc. ("Micron Semiconductor"), Micron Technology Texas LLC ("Micron Texas"), and all affiliates, related entities, parents, branches, subsidiaries or divisions, and any predecessor or successor entities and any of its officers, directors, agents, attorneys, consultants, accountants, employees, representatives, investigators, distributors, salespersons, sales representatives, licensors, licensees, and any other persons acting, or purporting to act for or on its or their behalf or under its or their control, including but not limited to experts or persons consulted concerning

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any factual matter or matters of opinion relating to any issues involved in the action.<sup>1</sup>

2. “Netlist” shall mean Netlist, Inc. and all of its affiliates, officers, employees, agents, representatives, contractors, consultants, attorneys, successors, and assigns.

3. “Netlist Patents-in-Suit” shall mean and refer to, both individually and collectively, U.S. Patent Nos. 10,860,506 (the “506 Patent”); 10,949,339 (the “339 Patent”); 11,016,918 (the “918 Patent”); 11,232,054 (the “054 Patent”); 8,787,060 (the “060 Patent”); and 9,318,160 (the “160 Patent”), as well as all applications and patents that share a common priority claim. The applications and patents that share a common priority claim include but are not limited to those listed in the table below:

<b>Country</b>	<b>Application Number</b>	<b>Publication Number</b>	<b>Patent Number</b>
US	16/391,151	2019-0347220	10,860,506
US	13/952,599	2014-0337539	9,128,632
US	14/846,993	2016-0034408	9,563,587
US	15/426,064	2017-0147514	9,824,035
US	15/820,076	2018-0095908	10,268,608
US	15/470,856	2017/0337125	10,949,339
US	12/504,131	2011-0016269	8,417,870
US	12/761,179	2011-0016250	8,516,185
US	13/970,606	2014-0040568	9,606,907
US	17/138,766	2021-0124701	11,016,918

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<sup>1</sup> In this letter, the term “including” means “including without limitation,” and the terms “and” and “or” are terms of inclusion and not of exclusion as appropriate, so as to bring within the scope of these examples all materials that might otherwise be construed to be outside of their scope. “Person” includes any natural person, firm, partnership, association, corporation, trust, and any other business, governmental or legal entity.

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<b>Country</b>	<b>Application Number</b>	<b>Publication Number</b>	<b>Patent Number</b>
US	17/328,019	2021-0279194	11,232,054
US	13/288,850	2012-010622	8,787,060
US	14/337,168	2015-0070959	9,318,160
US	15/095,288	2016-022541	9,659,601
US	15/602,099	2017-0256291	10,290,328

4. “Micron Accused DDR4 LRDIMMs” shall include any and all Micron Double Data Rate 4 (“DDR4”) load-reduced dual in-line memory modules (“LRDIMMs”), including ones that its customers further customize.

5. “Micron Accused DDR5 DIMMs” shall include any and all Micron Double Data Rate 5 (“DDR5”) dual in-line memory modules, including ones that its customers further customize.

6. “Micron Accused HBM Products” shall include any and all Micron HBM2, HBM2E, or HBM3 high bandwidth memory products, including ones that its customers further customize.

7. “Micron Accused Infringing Products” shall mean any and all Micron Accused DDR4 LRDIMMs, Micron Accused DDR5 DIMMs, and Micron Accused HBM Products.

8. “Micron Distributor” shall include any person who Micron authorized to sell any Micron Accused Infringing Products.

9. “Micron Partner” shall include any customers of Micron’s Accused Infringing Products and any other third parties involved in the design, development, manufacture, testing, assembly, importation, distribution, importation, sourcing, qualification, sale, or offer to sell Micron Accused Infringing Products, and any person who supplied, designed, manufactured, or sold any components or features of any Micron Accused Infringing Products, including but not limited to Montage, Rambus, Renesas, and Texas Instruments.

10. “Source Code” shall mean a complete copy of the referenced source codes for

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RTL code, firmware, middleware, or software.

11. “Third party” means any individual, entity, organization, partnership, or corporation that is not a party to this action.

### **Categories of Documents**

1. Product manuals, data sheets, application notes, specifications, brochures, and/or user guides for each Micron Accused Infringing Product.

2. Documents sufficient to identify all features, names, and codes for each Micron Accused Infringing Product.

3. Documents sufficient to fully describe the design and operation of each Micron Accused Infringing Product.

4. Circuit diagrams, design files, JEDEC reference designs, RTL code and/or software or firmware code of each Micron Accused Infringing Product sufficient to show the accused structures, functionality, and operation, including: (1) the write operation; (2) the read operation; (3) control and timing of the write buffer(s); (4) control and timing of the read buffer(s); (5) information sent during and after training mode; (6) chip selection generation and signaling; (7) rank multiplication; (8) on-board power management circuitry (including circuits for monitoring input voltages, regulating output voltages, voltage levels and sources for each component in a DRAM module, and signaling and register update in response to over-voltage or under-voltage conditions); (9) HBM layout, interconnections and signaling (including interconnections between TSVs and data/command/address drivers in DRAM dies, interconnections between TSV and signal lines/drivers in the logic die in a HBM, power supply to logic die and DRAM dies, and how a specific chip or channel is selected in a HBM); and (10) any other information relevant to each asserted claim, including those relevant to Micron’s non-infringement theories.

5. Representative samples for each Micron Accused Infringing Product.

6. Documents sufficient to show, for each version of design files, circuit diagrams, Source Code used in each Micron Accused Infringing Product, the version release date, and the date that version was put into service in each of these products.

7. Documents sufficient to identify each and all Micron Accused Infringing Products sold since June 10, 2016.

8. Documents related to analyst reports, industry surveys, and studies about the

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global market of each Micron Accused Infringing Product, including searches on specific attributes and competitive analyses of these markets, since June 10, 2016.

9. Documents relating to any product, service, or process that competes with each and all Micron Accused Infringing Products.

10. Documents sufficient to identify the date of first make, use, or sale of each Micron Accused Infringing Product.

11. Documents relating to any opinion letters, memoranda, study, investigation, search, analysis, or opinion about the validity, enforceability, scope, or infringement of the Netlist Patents-in-Suit, or any asserted claim of any Netlist Patents-in-Suit.

12. Documents sufficient to show the monthly volume of each Micron Accused Infringing Product sold, offered for sale, or made in the United States, imported into the United States, or exported from the United States.

13. All documents related to the requests for proposals seeking any bid for components of any Micron Accused Infringing Products sent by Micron's customers since June 10, 2016.

14. Documents, sales records, or other reports for the sales of each and all Micron Accused Infringing Products sufficient to demonstrate, on a transaction-by-transaction basis: (1) the identity of Micron's customer; (2) product name; (3) volume of sale; (4) shipping destination; (5) importation and/or shipping origin; (6) price; (7) discount; and (8) transaction date.

15. All studies, analyses, reports, or other documents relating to Micron's market shares for each Micron Accused Infringing Product.

16. All studies, analyses, reports, or other documents sufficient to demonstrate market dominance or other competitive advantages Micron acquired relating to the sales launch of Micron Accused Infringing Products.

17. Documents sufficient to describe Micron's decision to offer or not offer DDR5 products.

18. Documents sufficient to describe Micron's decision to offer or not offer HBM2, HBM2E, HBM3, and newer generations of HBM products.

19. Documents sufficient to identify Micron's key competitors in the DDR5

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market and the market share of each.

20. Documents sufficient to identify Micron's key competitors in the HBM2/HBM2E/HBM3 markets and the market share of each key competitor.

21. Documents sufficient to identify the closest non-infringing alternatives for each asserted claim.

22. Documents sufficient to demonstrate the benefits or advantages of each Micron Accused Infringing Product compared to its respective closest non-infringing alternatives that You identified in response to Netlist's RFP No. 21, including without limitation, any technical advantages and cost-saving benefits.

23. All studies, analyses, reports, or other documents in Micron's possession, control, or custody related to the operation of data buffers in Micron Accused DDR4 LRDIMMs, including simulations performed by Micron and/or third parties.

24. All Documents related to the configuration, implementation, or operation of the registering clock driver, data buffers, and DRAMs on each of the Micron Accused DDR4 LRDIMMs, including but not limited to features described in Netlist's P.R. 3-1 preliminary infringement contentions.

25. Documents sufficient to fully describe the operation of the data buffers in Micron Accused DDR4 LRDIMMs, including, but not limited to, documents related to how the data buffers in Micron Accused DDR4 LRDIMMs (1) generate a delayed read strobe; (2) determine the amount of delay; (3) sample the delayed read data using the delayed read strobe; and (4) transmit the read data to the data bus (Steps 1-4 collectively referred to as "LRDIMM Data Buffer Read Timing"). Such documents include, but are not limited to, circuit diagrams, design files, Source Code, application notes, specifications, datasheets, description of operation principles, functional block diagrams, and presentations of the relevant integrated circuits and components.

26. Software and firm code, RTL code, circuit diagrams, design files, data sheets, product specifications, product manuals, and other types of technical documents sufficient to show the presence or absence of the LRDIMM Data Buffer Read Timing feature in the Micron Accused DDR4 LRDIMMs.

27. Documents sufficient to fully describe all testing (and results of that testing) Micron did or commissioned others to do to ensure proper LRDIMM Data Buffer Read

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Timing in Micron Accused DDR4 LRDIMMs.

28. All documents relating to Micron's decisions to use a data buffer to control the timing of data signals in Micron Accused DDR4 LRDIMMs, including when such features were first included, what alternatives were/are available, why Micron included this feature in any Micron Accused DDR4 LRDIMMs, and who was involved in the decision making.

29. To the extent that You contend that any Micron DDR4 LRDIMM does not use "signals received by the first data buffer during one or more previous operations" to determine the "first predetermined amount," all documents relating to such contention.

30. Documents related to any analysis (including studies or expert evaluation) of the value of patents or patent rights relating to LRDIMM Data Buffer Read Timing.

31. Documents relating to any comparisons between the Netlist Patents-in-Suit and any implemented or proposed memory modules incorporating the LRDIMM Data Buffer Read Timing feature in Micron Accused DDR4 LRDIMMs.

32. Documents relating to advertisements, including marketing documents, sales documents, and internet web pages, made by or on behalf of You or Micron Distributors relating to benefits conferred by the LRDIMM Data Buffer Read Timing feature.

33. Documents, including license agreements and settlement agreements, related to the royalty rate and total royalties You charge or pay for the use, manufacture, or sale of technology or intellectual property, including patents, relating to the LRDIMM Data Buffer Read Timing feature in each Micron Accused DDR4 LRDIMM.

34. Documents related to the existence and content of any industry practice for royalties on intellectual property concerning the LRDIMM Data Buffer Read Timing in each Micron Accused DDR4 LRDIMM.

35. Documents related to JEDEC discussions regarding the incorporation of LRDIMM Data Buffer Read Timing in DDR4 LRDIMMs, including the alternatives discussed.

36. All studies, analyses, reports, or other documents related to the configuration, implementation, or operation of the enablement/disablement of write or read buffers in Micron Accused DDR4 LRDIMMs, including simulations performed by Micron and/or third parties.

37. Documents sufficient to fully describe the enablement/disablement of read or write buffers in Micron Accused DDR4 LRDIMMs, including, but not limited to, documents



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related to: (1) software or hardware components in the Accused Instrumentality involved in controlling the write or read buffers; (2) signals involved in controlling the write or read buffers; (3) components that generate and/or receive the signals identified in (2); and (4) the time period during which the write or read buffers are enabled or disabled. (Features 1-4 collectively referred to as (“LRDIMM Write/Read Buffer Control”). Such documents include, but are not limited to, circuit diagrams, design files, Source Code, application notes, specifications, datasheets, descriptions of operation principles, functional block diagrams, and presentations of the relevant integrated circuits and components.

38. Software and firm code, RTL code, circuit diagrams, design files, data sheets, product specifications, product manuals, and other types of technical documents sufficient to show the presence or absence of enablement/disablement of write or read buffers in Micron Accused DDR4 LRDIMMs.

39. Documents sufficient to fully describe all testing (and results of that testing) Micron did or commissioned others to do to ensure proper timing of the enablement/disablement of write or read buffers in Micron Accused DDR4 LRDIMMs.

40. All documents relating to Micron’s decisions to use timed enablement/disablement of write or read buffers in Micron Accused DDR4 LRDIMMs, including when such features were first included, what alternatives were/are available, why Micron includes this feature in all Micron Accused DDR4 LRDIMMs, and who was involved in the decision making.

41. Documents related to any analysis (including studies or expert evaluation) of the value of patents or patent rights relating to the timed enablement/disablement of write or read buffers in Micron Accused DDR4 LRDIMMs.

42. Documents relating to any comparisons between the Netlist Patents-in-Suit and any implemented or proposed memory modules incorporating the timed enablement/disablement of write or read buffers in Micron Accused DDR4 LRDIMMs.

43. Documents relating to advertisements, including marketing documents, sales documents, and internet web pages, made by or on behalf of You or Micron Distributors relating to benefits conferred by the timed enablement/disablement of write or read buffers.

44. Documents, including license agreements and settlement agreements, related to the royalty rate and total royalties You charge or pay for the use, manufacture, or sale of technology or intellectual property, including patents, relating to the enablement/disablement

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of read or write buffers in each Micron Accused DDR4 LRDIMM.

45. Documents related to the existence and content of any industry practice for royalties on intellectual property concerning the enablement/disablement of read or write buffers in each Micron Accused DDR4 LRDIMM.

46. Documents related to JEDEC discussions regarding the incorporation of the timed enablement/disablement of read or write buffers in DDR4 LRDIMMs, including the alternative discussed.

47. Documents sufficient to identify Micron engineers who participated in JEDEC discussions related to the timed enablement/disablement of read or write buffers.

48. All studies, analyses, reports, or other documents in Micron's possession, control, or custody related to implementing the power management circuitry (including voltage regulation and monitoring circuitry) on the module board instead of on the motherboard in Micron Accused DDR5 DIMMs, including simulations performed by Micron and/or third parties.

49. All Documents related to the configuration, implementation, or operation of any power management integrated circuit ("PMIC"), buck converters, linear voltage regulators, voltage regulation and monitoring modules, or similar circuit components in Micron Accused DDR5 DIMMs, including those described in Netlist's P.R. 3-1 preliminary infringement contentions.

50. Documents sufficient to fully describe the power management and voltage regulation and monitoring in Micron Accused DDR5 DIMMs, including, but not limited to, documents related to how PMIC(s) in Micron Accused DDR5 DIMMs (1) produce regulated voltages; (2) monitor power input voltage; (3) respond to changes in power input voltage (e.g., an over-voltage or under-voltage condition); and (4) write information to non-volatile memory in response to changes in power input voltage. Such documents include, but are not limited to, circuit diagrams, design files, Source Code, application notes, specifications, datasheets, descriptions of operation principles, functional block diagrams, and presentations of the relevant integrated circuits and components.

51. Software and firm code, RTL code, circuit diagrams, design files, data sheets, product specifications, product manuals, and other types of technical documents sufficient to show the presence or absence of circuitry on the module board in Micron Accused DDR5 DIMMs that regulates and monitors voltage input to the DIMM and to components on the DIMM, and registers whose content is updated in response to over-voltage or under-voltage

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conditions (and how the update is done).

52. Documents sufficient to fully describe all testing (and results of that testing) Micron did or commissioned others to do to ensure the proper implementation of power management circuitry on the module board in Micron Accused DDR5 DIMMs.

53. All documents related to Micron's decision to implement the power management circuitry (including voltage regulation and monitoring circuitry) on the module board instead of on the motherboard in Micron Accused DDR5 DIMMs, including when such features were first included, what alternatives were/are available, why Micron includes this feature in any Micron Accused DDR5 DIMMs, and who was involved in the decision making to include these features.

54. All documents related to the industry's discussion regarding the pros and cons of implementing the power management circuitry (including voltage regulation and monitoring circuitry) on the module board instead of on the motherboard in Micron Accused DDR5 DIMMs.

55. RTL code, software or firmware code, circuit diagrams, design files, functional diagrams, data sheets, product specifications, product manuals, and other technical documents related to the power management circuitry (including voltage regulation and monitoring circuitry) on the module board in each Micron Accused DDR5 DIMM.

56. RTL code, software or firmware code, circuit diagrams, design files, functional diagrams, data sheets, product specifications, product manuals, and other technical documents related to PMIC register update and write operation in response to over-voltage or under-voltage detection in each Micron Accused DDR5 DIMM.

57. To the extent that You contend that any Micron DDR5 DIMM does not include a voltage conversion circuit with "at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages," all documents relating to such contention.

58. To the extent that You contend that any Micron DDR5 DIMM does not include "a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude," all documents relating to such contention.

59. Documents related to any analysis (including studies or expert evaluation) of the value of patents or patent rights relating to implementing the power management circuitry

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on the module board instead of on the motherboard in each Micron Accused DDR5 DIMM.

60. Documents relating to any comparisons between the Netlist Patents-in-Suit and any implemented or proposed memory modules incorporating on-module power management circuitry as in Micron Accused DDR5 DIMMs.

61. Documents relating to advertisements, including marketing documents, sales documents, and internet web pages, made by or on behalf of You or Micron Distributors relating to benefits conferred by implementing the power management circuitry on the module board instead of on the motherboard.

62. Documents, including license agreements and settlement agreements, related to the royalty rate and total royalties You charge or pay for the use, manufacture, or sale of technology or intellectual property, including patents, relating to implementing the power management circuitry on the module board instead of on the motherboard in each Micron Accused DDR5 DIMM.

63. Documents related to the existence and content of any industry practice for royalties on intellectual property concerning implementing the power management circuitry on the module board instead of on the motherboard in each Micron Accused DDR5 DIMM.

64. Documents related to JEDEC discussions regarding implementing the power management circuitry on the module board instead of on the motherboard in DDR5 DIMMs, including the alternatives discussed.

65. Documents sufficient to identify Micron engineers who participated in JEDEC discussions regarding implementing the power management circuitry on the module board instead of on the motherboard.

66. All studies, analyses, reports, or other documents in Micron's possession, control, or custody related to the transmission of data, control, and address signals from the host (e.g., a CPU, GPU, or SoC) to the control die (e.g., buffer die or logic die) or the DRAM dies in Micron Accused HBM Products, including simulations performed by Micron and/or third parties.

67. All Documents related to the configuration, implementation, or operation of the control die (e.g., buffer die or logic die) in Micron Accused HBM Products, including those described in Netlist's P.R. 3-1 preliminary infringement contentions.

68. Documents sufficient to fully describe the HBM layout, interconnections, and signaling in Micron Accused HBM Products, including, but not limited, to documents related

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to: (1) how Micron Accused HBM Products communicate data, control, and address signals with one or more external devices (e.g., a CPU, GPU, or SoC of the host); (2) how Micron Accused HBM Products communicate data, control, and address signals to and from a particular DRAM in the stack; (3) the configuration and interconnections of the die interconnects (e.g. TSVs) in Micron Accused HBM Products; (4) how Micron Accused HBM Products electrically isolate or reduce the load presented by the die interconnects (e.g., TSVs); (5) interconnections between TSVs and drivers in the DRAM dies; (6) interconnections between TSVs and drivers in the control die (e.g., buffer die or logic die); (7) the determination of the driver size for data conduits in the control die; and (8) interconnections between TSVs in DRAMs and I/O and power terminals. Such documents include, but are not limited to, circuit diagrams, design files, Source Code, application notes, specifications, datasheets, descriptions of operation principles, functional block diagrams, and presentations of the relevant integrated circuits and components.

69. Software and firm code, RTL code, circuit diagrams, design files, data sheets, product specifications, product manuals, and other types of technical documents sufficient to show the presence or absence of data drivers in the control die (e.g., buffer die or logic die) and the DRAM dies in Micron Accused HBM Products.

70. Documents sufficient to fully describe all testing (and results of that testing) Micron did or commissioned others to do to ensure proper communication of data, control, and address signals to the control die (e.g., buffer die or logic die) and the DRAM dies in Micron Accused HBM Products.

71. All Documents relating to the die interconnects' interconnections in 4-stack HBM2/HBM2E/HBM3s versus 8- and 12-stack HBM2/HBM2E/HBM3s versus 16-stack HBM3s.

72. Documents related to any analysis (including studies or expert evaluations) of the value of patents or patent rights relating to the die interconnection configurations.

73. Documents relating to any comparisons between the Netlist Patents-in-Suit and any implemented or proposed memory modules incorporating die interconnects that are in electrical communications with some DRAM dies, but not other DRAM dies in Micron Accused HBM Products.

74. Documents relating to advertisements, including marketing documents, sales documents, and internet web pages, made by or on behalf of You or Micron Distributors relating to benefits conferred by the use of die interconnects that are in electrical

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communication with some DRAM dies but not others.

75. Documents, including license agreements and settlement agreements, related to the royalty rate and total royalties You charge or pay for the use, manufacture, or sale of technology or intellectual property, including patents, relating to Micron Accused HBM Products.

76. Documents related to the existence and content of any industry practice for royalties on intellectual property concerning HBM products.

77. Documents related to JEDEC discussions regarding specifying communication of data, control, and address signals to the control die (e.g., buffer die or logic die) and the DRAM dies in high bandwidth memory products, including the alternatives discussed.

78. Documents sufficient to identify Micron engineers who participated in JEDEC discussions related to specifying communication of data, control, and address signals to the control die (e.g., buffer die or logic die) and the DRAM dies in HBM products.

79. Agreements between Micron and its customers, including master sales agreements, master service agreements, statements of work, purchase orders, invoices, delivery notices, and export/import documentation.

80. Documents, including internal and external monthly, quarterly, and annual financial statements, profit and loss reports, studies of profitability, gross margin, turnover, price lists and price books, quotations, tax returns, and other related documents sufficient to determine, for each Micron Accused Infringing Product, total gross and net revenues, total average monthly revenue per device, fixed costs, variable costs, cost of goods sold, selling, general, and administrative (“SGA”) expenses, variance from standard costs, gross and net profits, any non-standard costs or expenses, and accounting methods used with respect to the Micron Accused Infringing Products.

81. Documents sufficient to fully describe any contract negotiation or contract performance regarding the purchase, sale, manufacture, or assembly of each Micron Accused Infringing Product, including, but not limited to: (1) identity of each and all parties involved; (2) locations where any contract, pricing, and projected demand were negotiated and executed; (3) where requests for proposal or bids are submitted; (4) location where each Micron Accused Infringing Product was shipped from; (5) location where each Micron Accused Infringing Product was shipped to; (6) location where title of each Micron Accused Infringing Product was transferred or other locations where Micron and the purchaser agreed that a transfer would take place; (7) billing addresses; (8) locations where each Micron Accused Infringing Product

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was manufactured, assembled, and tested; and (9) identity of individuals responsible for contract negotiation.

82. Agreements between You and Your customers for delivery and/or manufacture of each Micron Accused Infringing Product, including but not limited to contracts, documents memorializing such agreements, statements of work, purchase orders, invoices, instructions for a specific delivery or manufacture, master service agreements, master purchase agreements, joint development agreements, and requests for bids and bids submitted in response. The Micron Accused Infringing Products include not only products delivered to the customers but also products (even if not completely finished) that You deliver to a contractor or an agent of the customers for further processing.

83. Documents relating to any market forecasts concerning sales or usage of each Micron Accused Infringing Product, whether by Micron, any competitor or potential competitor, or any Micron Distributor, including market forecasts relating to: potential sales, profits, costs, cost comparisons, competitor analyses, market shares, customer surveys, intellectual property protection, or product or service strategies.

84. Documents related to budgets for the development, manufacture, assembly, testing, sale, use, or lease of each Micron Accused Infringing Product.

85. Documents related to any meeting or other conference between You and stock, financial, or similar analysts at which any Micron Accused Infringing Product was discussed.

86. Documents relating to any calculation of expected or actual attachment rates, relationships, or sales ratios between Micron Accused Infringing Products sales and Your conveyed sales, derivative sales, follow-on sales, tag-along sales, or any other sales made with any of these products.

87. Documents relating to advertisements, including marketing documents, sales documents, and internet web pages, made by or on behalf of You or Micron Distributors relating to Micron Accused Infringing Products.

88. Agreements between You and Micron Distributors (including contracts or documents memorializing such agreements) or documents sufficient to show the quantity and content of such agreements.

89. Documents sufficient to demonstrate the identity of and the specific role played by each Micron Partner involved in the design, research, development, manufacture, assembly, testing, use, distribution, advertisement, marketing, sale, and offer for sale of each



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**Micron Accused Infringing Product.**

90. For each Micron Accused Infringing Product made overseas, identify the person(s) or entities who imported the products into the United States (even if the products were later exported).

91. For each Micron Accused Infringing Product made overseas, identify the location at which the Product was contemplated to be delivered and the location at which the Product was actually delivered.

92. Agreements between You and Micron Partners (including contracts or documents memorializing such agreements) related to the supply, manufacture, or assembly of components in each Micron Accused Infringing Product.

93. Documents related to any analysis of the value of patents or patent rights owned by Netlist.

94. Documents related to Micron's suggested retail prices for each Micron Accused Infringing Product.

95. Documents related to any determination by Micron or Micron Partners of the pricing or suggested pricing of each Micron Accused Infringing Product.

96. Documents sufficient to show the location of manufacture for components in each Micron Accused Infringing Product.

97. Documents sufficient to describe any Netlist patent or patent application that Micron is aware of and the circumstances under which Micron has become aware of the patent or patent application.

98. Organizational charts or similar documents relating to the organization or location of any facility or group involved in the design, research, development, implementation, or manufacture of Micron Accused Infringing Products.

99. Documents sufficient to determine the name, location, title, and role of all employees involved in the design, research, development, implementation, or manufacture of components or technology used for each Micron Accused Infringing Product.

100. Documents sufficient to determine the name, location, title, and role of all employees involved in the marketing, sale, or distribution of each Micron Accused Infringing



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Product.

101. Documents sufficient to show the structure of the sales and marketing departments, distributor relationships, distribution system, total market coverage, sales force territories, sales force numbers, or compensation and commission structures related to each Micron Accused Infringing Product.

102. Documents sufficient to show who at Micron became aware of the existence of the Netlist Patents-in-Suit before the initiation of this lawsuit and when and how this occurred.

103. Documents sufficient to describe any Netlist memory designs that Micron has received or is aware of and the circumstances under which Micron has received or become aware of the designs.

104. Documents sufficient to describe any Netlist requests for bids that Micron has received or is aware of and the circumstances under which Micron has received or become aware of the requests.

105. Documents relating to actions that You took upon becoming aware of the existence of the Netlist Patents-in-Suit, including documents relating to risk or damages analysis of potential infringement of any of the Netlist Patents-in-Suit.

106. Communications between You and Google LLC and/or Google LLC's supplier or contractor concerning Netlist, Netlist Patents-in-Suit, or any litigation or other proceeding involving Netlist.

107. Documents sufficient to identify Micron engineers who participated in JEDEC discussions related to the LRDIMM Data Buffer Read Timing feature.

108. Documents sufficient to identify each alternative that JEDEC considered before adopting the sections of the specifications referenced in Netlist's preliminary infringement contentions.

109. Documents sufficient to describe Micron's participation in JEDEC, including its evaluation of proposals submitted by its competitors (including Netlist) to JEDEC, its decisions to support or not support the competitors' (including Netlist's) proposals, and its efforts to block or support the competitors' (including Netlist's) proposals.

110. Documents sufficient to identify instances where Micron did or did not offer

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a RAND license to an implementer for patents necessary to practice a JEDEC specification.

111. Documents sufficient to identify each instance where Micron did not offer a RAND and/or FRAND license because the implementer purportedly failed to negotiate in good faith negotiation of the license.

112. Correspondences between Micron and JEDEC as related to RAND commitments, including Micron's interpretation of what is required under the RAND obligations and when a third party beneficiary has forfeited the right to enforce the RAND obligation.

113. Any article, announcement, corporate policy, position paper, memorandum, correspondence, letter, or email by Micron as related to RAND commitments, including Micron's interpretation of what is required under the RAND obligations and when a third party beneficiary has forfeited the right to enforce the RAND obligation.

114. Any article, announcement, corporate policy, position paper, memorandum, correspondence, or letter by JEDEC in Micron's possession, control, or custody as related to RAND commitments, including Micron's interpretation of what is required under the RAND obligations and when a third party beneficiary has forfeited the right to enforce the RAND obligation.

115. Documents sufficient to describe Micron's decision to incorporate the power management and voltage regulation modules onto the DDR5 modules' printed circuit boards.

116. Studies and evaluations performed by Micron or third parties related to performance improvement or cost savings by incorporating the power management and voltage regulation modules onto the DDR5 modules' printed circuit boards.

117. Studies and evaluations performed by Micron or third parties on whether TSVs for signals should be selectively connected to only selected drivers in a selected subset of DRAM chips or to be connected to all DRAM chips.

118. Studies and evaluations performed by Micron or third parties on whether drivers for different TSVs should have the same size or different sizes.

119. Studies and evaluations performed by Micron or third parties on how to best determine the amount of delay for a read strobe by a data buffer in a DDR4 LRDIMM.

120. Studies and evaluations performed by Micron or third parties on how to determine the period, if any, during which tristate buffers are enabled to drive write data from

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a data buffer to a corresponding DRAM.

121. Studies and evaluations performed by Micron or third parties on whether to have the write drivers in a DDR4 LRDIMM's data buffer be enabled only for a selected period.

122. Documents sufficient to describe Micron's due diligence, study, and evaluation of its competitors' patent portfolio, in particular as related to DDR5, DDR4 LRDIMM, and HBMs.

123. Documents sufficient to describe Micron's due diligence, study, and evaluation of Netlist's patent portfolio, in particular as related to DDR5, DDR4 LRDIMM, and HBMs.

124. Documents related to Micron's knowledge of Netlist's DRAM designs.

125. Documents that relate to, discuss, or mention Netlist or its past or present directors, officers, agents, representatives, employees, consultants, attorneys, or others acting on its behalf.

126. Documents upon which You rely, or intend to rely, to support the position that Your infringement of the Netlist Patents-in-Suit is not deliberate or willful.

127. Documents relating to any comparisons between the Netlist Patents-in-Suit and any technology incorporated into each Micron Accused Infringing Product.

128. Documents relating to communications between You and any third party concerning the Netlist Patents-in-Suit or Netlist.

129. Communications, and related documents, between You and any person relating to any litigation or other proceeding involving the Netlist Patents-in-Suit, including communications with any person You may or will call or have called as a witness, may or will depose or have deposed at a deposition, or may or will defend or have defended at a deposition, in any litigation or other proceeding involving the Netlist Patents-in-Suit.

130. All documents constituting or relating to an alternative or design-around for a feature of any Micron Accused Infringing Product relating to Netlist Patents-in-Suit or this Action.

131. All documents, including meeting agendas, meeting minutes, internal memoranda, newsletters, presentations, emails, and other documents of Micron's board of directors, board committees, subcommittees, engineering, programming, management, legal,

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business development, or sales and marketing personnel, referring to or relating to the Netlist Patents-in-Suit, Netlist, or any litigation or other proceeding involving Netlist.

132. Documents concerning any litigation or other proceeding relating to any alleged Prior Art to the Netlist Patents-in-Suit.

133. Alleged Prior Art to the Netlist Patents-in-Suit.

134. To the extent You contend that Netlist's Patents-in-Suit are essential to any standards set by any standard-setting organization, documents sufficient to show the relevant standard(s).

135. To the extent You contend that Netlist's Patents-in-Suit are essential to any standards set by any standard-setting organization, documents sufficient to show discussions that led to the adoption of the technical features at issue in Netlist's Patents-in-Suit.

136. To the extent You contend that Netlist's Patents-in-Suit are essential to any standards set by any standard-setting organization, documents sufficient to show Micron's participation in discussions that led to the adoption of the technical features at issue in Netlist's Patents-in-Suit.

137. To the extent You contend that Netlist's Patents-in-Suit are essential to any standards set by any standard-setting organization, documents sufficient to show alternatives that the standard-setting organization considered before adopting the features at issue in Netlist's Patents-in-Suit.

138. To the extent You contend that Netlist's Patents-in-Suit are essential to any standards set by any standard-setting organization, provide a full list of patents that cover the same technical features at issue in Netlist's Patents-in-Suit and when each was declared.

139. Documents sufficient to identify patents that You contend are essential to the implementation of DDR4 LRDIMMs and when each was declared.

140. Documents sufficient to identify patents that You contend are essential to the power management and voltage regulation/monitoring function in DDR5 and when each was declared.

141. Documents sufficient to identify the patents You contend are essential to high bandwidth memory products and when each was declared.

142. To the extent You contend that Netlist's Patents-in-Suit are essential to any

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standards set by any standard-setting organization, all documents relating to Micron's disclosures, declarations, or RAND offers submitted to the standard-setting organization in connection with the standards relevant to Netlist's Patents-in-Suit, including but not limited to the standards cited in Netlist's P.R. 3-1 preliminary infringement contentions.

143. Documents sufficient to identify RAND rates that Micron has offered on patents related to DDR4 LRDIMM and DDR5 products.

144. Documents sufficient to identify the number of patents owned by Micron that Micron contends are essential to DDR4 LRDIMM and DDR5.

145. All non-privileged Documents in Micron's possession relating to Netlist Patents-in-Suit.

146. Documents produced in response to any subpoena issued by or to You in connection with any litigation or other proceeding involving the Netlist Patents-in-Suit.

147. Press releases or drafts thereof, discussing the Netlist Patents-in-Suit, Netlist, or any litigation or other proceeding involving Netlist.

148. Documents related to communications between You and any consultant or advisor retained by or on behalf of Micron or any other party relating to any litigation or other proceeding involving Netlist or the Netlist Patents-in-Suit, including documents relied on or considered by said consultant.

149. Documents related to Micron's evaluation of damages in actions involving DRAM patents, including expert reports, deposition transcripts, and trial testimony.

150. Documents relating to Your document retention or destruction policies or practices.

151. Documents related to Your corporate policy or procedures, whether formal or informal, on licensing Micron's technology, including its patents, or on use, non-use, or licensing of technology claimed in patents owned by or assigned to entities other than You.

152. Documents relating to Micron's participation in JEDEC, especially as relating to features introduced to DDR4 LRDIMMs, DDR5 power management, HBM2, HBM2E, and HBM3.

153. Documents relating to Micron's policy on standards for determining essential patents, including the process by which You determine which patents should be declared to

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JEDEC and when.

154. Documents sufficient to identify people responsible for deciding which of Micron's patents or patent applications should be declared to JEDEC and when those declarations should be made.

155. Documents relating to Micron's declaration of patents allegedly essential to JEDEC standards.

156. Correspondences between Micron and JEDEC concerning DDR4 LRDIMMs, DDR5 DIMMs, HBM2, HBM2E, and HBM3.

157. RAND assurance letters or refusal-to-license letters from Micron to JEDEC and any related correspondences and documents.

158. Correspondences between Micron and other JEDEC members concerning DDR4 LRDIMMs, DDR5 DIMMs, HBM2, HBM2E, and HBM3.

159. Correspondences between Micron and its customers concerning DDR4 LRDIMMs, DDR5 DIMMs, HBM2, HBM2E, and HBM3.

160. Correspondences between Micron and its suppliers concerning DDR4 LRDIMMs, DDR5 DIMMs, HBM2, HBM2E, and HBM3.

161. Correspondences between Micron and its competitors (including Samsung and Hynix) concerning DDR4 LRDIMMs, DDR5 DIMMs, HBM2, HBM2E, and HBM3.

162. Correspondences between Micron and any third parties concerning DDR4 LRDIMMs, DDR5 DIMMs, HBM2, HBM2E, and HBM3.

163. All Documents supporting or identified in response to Netlist's interrogatories served in this action.

In accordance with Your obligations under the Discovery Order and the Federal and Local Rules, Micron must produce all relevant documents, materials, tangible things, and information, including but not limited to the examples listed above.

**I R E L L   &   M A N E L L A   L L P**  
A REGISTERED LIMITED LIABILITY LAW PARTNERSHIP  
INCLUDING PROFESSIONAL CORPORATIONS

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Very truly yours,

/s/ Yanan Zhao  
Yanan Zhao

cc: Counsel of Record (per agreed service emails)